Development of the SCORR Process System for the mass production of 300mm Semiconductor Wafer

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Abstract

The semiconductor device makers are processing the 300mm wafers and fabricating 40nm node semiconductor devices these days, and also 20nm node semiconductor devices will be fabricated sooner or later. Wet stripping and cleaning methods that employing huge amount of ultrapure water and toxic chemicals in semiconductor industry are confronted with serious triple problems such as environmental, economical and technological limitation for further use as the pattern becomes nanoscale. It is mainly due to the fact that water has undesirable high surface tension, high viscosity and low diffusivity. The surface tension of IPA(isopropyl alcohol) which is mainly used for drying solvent in the conventional dry method is 22dyne/cm. Although new solvent is applied, it is not possible to lower 11dyne/cm and below. So, conventional drying solvents lead to pattern collapse by the stiction between patterns on the sub-30nm node semiconductor devices having high aspect ratio. For solving the above mentioned problems, the SCORR(*Supercritical Carbon Dioxide Resist Removal*) process has been developed by authors during the last several years. Especially when this SCORR equipment system is applied for mass production of semiconductor devices, the core issues such as methods of rapid and stable feeding of supercritical fluids, stable and long term sealing, continuous and rapid automatic chamber open/close, continuous and stable wafer loading/unloading and the recycling of a great quantity of CO2 that have been internationally discussed for a long time must be solved. Those core issues were able to be solved through this work. Thus, in the present work, the efforts they made from laboratory work to commercialization of the SCORR system will be discussed. Based on the good results from the efforts on this work, it was found that the SCORR system demonstrated here can be a practical alternative for replacing wet-cleaning stations in semiconductor fabrication line in the near future.

Keywords : SCORR; sc-CO_2; supercritical carbon dioxide; 300mm wafer; nano-pattern;
Additive; Homogeneous and transparent phase; sc-CO_2 Drying;
Pattern collapse; pattern leaning; CO_2 recycle system

1. Introduction

This study is related to the development of dry cleaning process based on supercritical carbon dioxide(sc-CO_2), and commercial-version SCORR and CO_2 recycle system for cleaning 300mm nano-pattern wafer. Generally PR(photoresist) and its residues have to be removed from FEOL(front-end-of-line) and BEOL(back-end-of-line) wafers after ion implantation and etching, but there is some difficulty in requiring to do so. To thoroughly remove photoresist and its residues, semiconductor companies typically use a combination of dry methods (plasma-based ashers) and wet methods (wafer cleaning tools). High temperature hard bakes, plasma etch/ash residues, sidewall polymers in contact holes and electrical interconnect trenches, ion implantation crust, shrinking feature size, all has the difficulty in removing the PR and its residues. In a conventional semiconductor device manufacturing process, a PR pattern is formed on a conductive layer which has been formed on a semiconductor substrate. The conductive layer whose portion is not covered by the pattern is etched using the PR pattern as a mask to form a conductive layer pattern. This lithography process is then repeated to form the conductive patterns. The PR pattern is used as the mask and it should be removed from the conductive layer in a stripping process after the process for forming the conductive layer pattern is completed. However, it is difficult to remove PR material in the subsequent stripping process since etching process for forming a conductive layer pattern is formed with a dry etching process when making highly integrated devices and, as a result, the physical property of PR is deteriorated during the dry etching process. During dry etching process, ions and radicals included in the plasma etching gas cause a complicated chemical reaction on the surface of a PR film which rapidly hardens the PR material. Specifically, when the dry etching process is performed on metal conductive layers such as aluminum films, titanium films and titanium nitride films, PR polymers on sidewalls of the metal conductive layer are chemically transformed and hardened. Since the PR materials are exposed to plasma gas in dry etching or ashing processes which are used for manufacturing ultra high integrated circuits, it is difficult to remove the PR material. Especially, ashing process performed after etching process is conventionally heated at a high temperature of over 200^{o}C. Here, residual solvent in the PR material should be vaporized and exhausted. However, a hardened PR layer which remains on the metal lines after the ashing process prevents exhaustion of the residual solvents. As a result, the surface of the PR film can be cracked by the residual solvent as internal pressure of the PR film increases during the ashing process. Since the hardened PR layer shattered by the ashing process still remains on metal lines, it is difficult to remove the PR material which is transformed into residues and particles. Such PR material may become polluters and causes to lower yield rate in manufacture of ultra high integrated circuits. When the ashing process is performed before the stripping process to remove the PR material, the transformation of the PR layer is deteriorated, which results in defects during the conventional water-based stripping process.

And also it has been known that it is difficult to remove the ion implanted PR on post-ion implanted wafer[5,6] because the implant species can penetrate into the PR, driving out hydrogen to form a crust of hardened, carbonized PR which has nonporous structure. It is difficult to remove the ion implanted PR using liquid solvents that can't easily penetrate into the carbonized layer, because of the surface tension problem. And when a conventional high-temperature plasma ashing strip process is applied, the heating of the damaged PR results in volatilization of resist solvent trapped underneath the crust layer, which builds up pressure and causes the carbonized crust layer to rupture, or popping [1]. As a result, the carbon dioxide based stripping method called SCORR was needed as a new technology[7,8]. SCORR method makes possible to clean semiconductor device effectively using only 1 step of sc-CO_2 strip, not conventional 2 step of plasma ash and wet clean. It must be introduced cleaning additives and rinsing additives including polar co-solvents to remove PR and its residues completely in supercritical fluids dry cleaning system. It is very important to keep one phase during cleaning and rinsing in order to remove PR residues and cleaning additives. So cleaning additives must be especially included amphiphilic surfactants which have CO_2-philic groups and CO_2-phobic (co-solvents-philic) group[2,3,4]. In this study, we formulated proper cleaning additives including surfactants for effective cleaning, and developed commercial-version SCORR and solvent recycle system for cleaning 300mm wafer like PR-hard baked wafer, BEOL wafer, and post-ion-implanted wafer and only drying 300mm wafer like 20nm-class NAND flash pattern wafer.

2. Materials and methods

2.1 Materials and analyses

The purity of carbon dioxide used was 99.95% and various kinds of fluorinated surfactants and solvents were used. The equipment is located in a clean room which has air-cleaner facilities. The wafers for SCORR test were used PR hard baked wafer, BEOL wafer which represent Al/SiO_2 circuit pattern, and arsenic(As) implanted wafers which were implanted under condition of energy of 60KeV and arsenic dose of 5E15/cm^2, and energy of 80KeV and arsenic dose of 1E13/cm^2. The wafers for sc-CO_2 Drying test were used 20nm-class NAND flash memory pattern wafer. In order to analyze the wafers surface, SEM(scanning electron microscope) was used before and after the experiment.

2.2 Process

The SCORR system developed for the mass production of 300mm semiconductor wafers is classified into main chamber system of commercial-version and CO_2 recycle system which is able to recycle a large quantity of CO_2. And whole process is progressing through a 5 step process (pressurizing, cleaning or stripping, rinsing, drying or CO_2 exhaust, and CO_2 recycle) continuously and automatically.

3. Results

SCORR test was carried out with pattern wafer samples like PR-hard baked wafer, BEOL wafer, and post-ion-implanted wafer. It was found that sc-CO_2 mixtures were made by mixing additives and sc-CO_2 should form HTP(homogeneous and transparent phase) in order to effectively and uniformly remove the hard baked PR, post-metal etch/ash PR and post ion-implanted PR from the wafers. The additives were formulated by mixing and co-solvents like an amine compound and fluoro-surfactants used as HTP agents, and the denatured PR and its residues on the wafer were able to be rapidly and effectively removed using the sc-CO_2 mixture of HTP. In this study, the SCORR process for the removal of denatured PR and its residues on the FEOL and BEOL wafers was proposed, which was able to rapidly form the sc-CO_2 mixture of HTP and maintains supercritical HTP during whole process, and the experimental results were explained by visual observation of the state of sc-CO_2 mixture, measuring the cloud points of them and inspection of the fine structure on ion-implanted wafer with SEM.

Good SCORR results were obtained from various tests for removing hard baked PR on FEOL wafer, post metal etch/ash PR residue on BEOL wafer, and ion implanted PR on post-ion implanted wafer.

The tests were carried out at 40~80? and 13~25Mpa. It was found that approximately 50bar larger than pressure of the cloud point measured was needed to completely and uniformly remove the denatured PR and its residues from the various wafers while maintaining HTP stably at the stripping temperature range from 40 to 80^{o}C. The PR and its residues on the various wafers could be removed effectively within 5 minutes.

Additionally, sc-CO_2 drying test were performed for the removal of DIW(de-ionized water) which were being used as rinsing agent without pattern collapse. The wafer used for sc-CO_2 drying was 20nm-class NAND flash memory pattern wafer, and the used sc-CO_2 mixture was mixture of sc-CO2 and appropriate drying agent. The tests were carried out at 50~80? and 10~13Mpa, and no pattern collapse(or pattern leaning) was not found after drying.

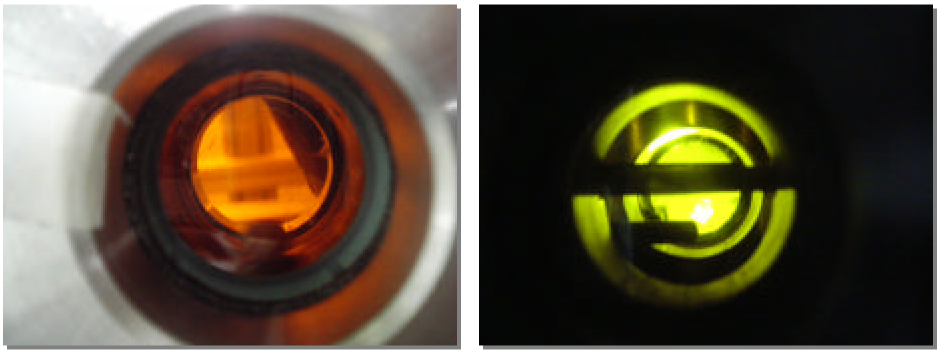
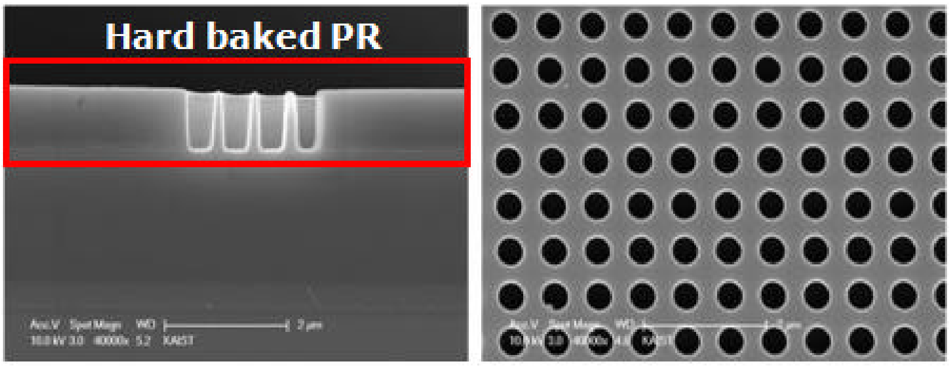
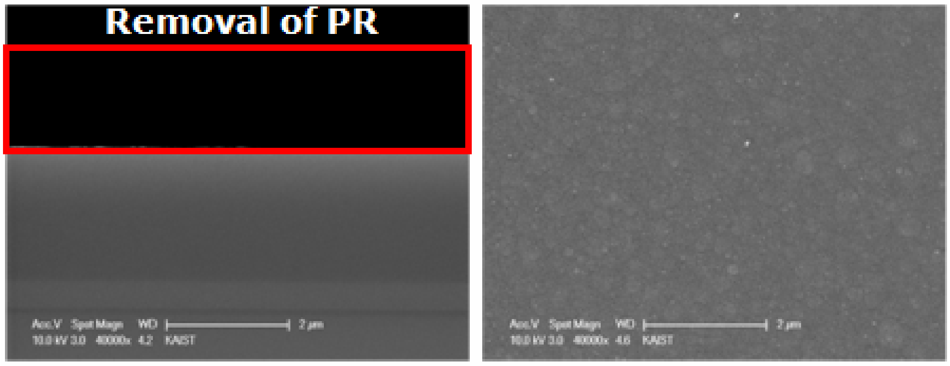


Figure 1. Examples of HTP mixture for cleaning

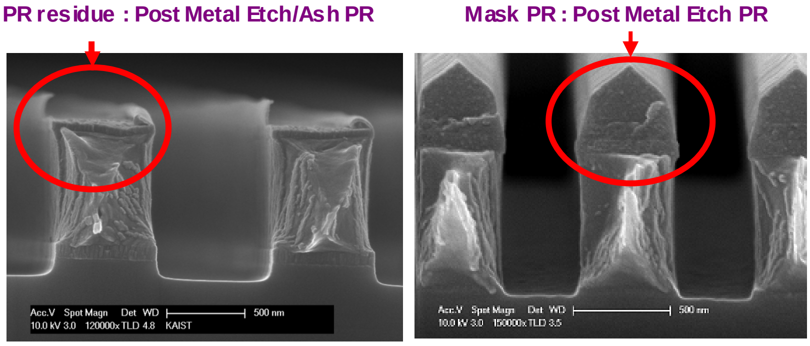


(2-a) Before cleaning of PR hard baked wafer

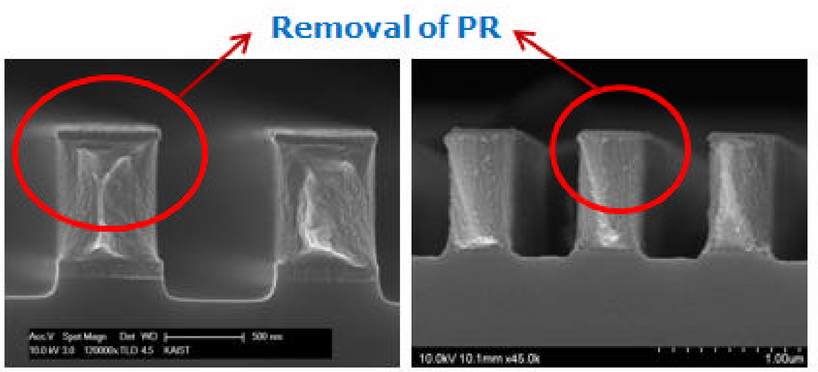


(2-b) After cleaning of PR hard baked wafer

Figure 2. The SCORR result of PR hard baked wafer

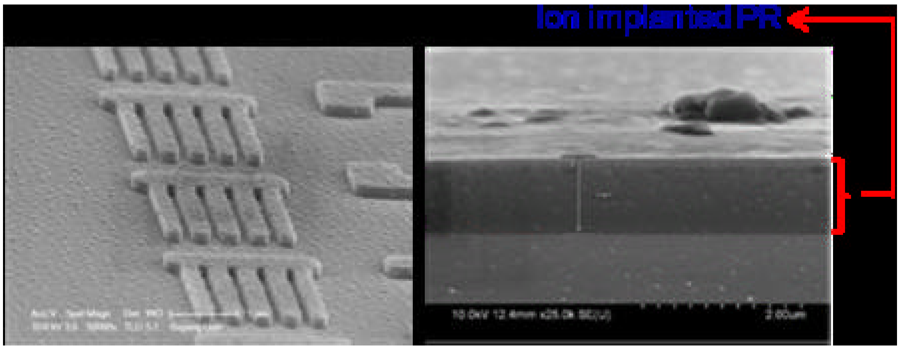


(3-a) Before cleaning of BEOL wafer

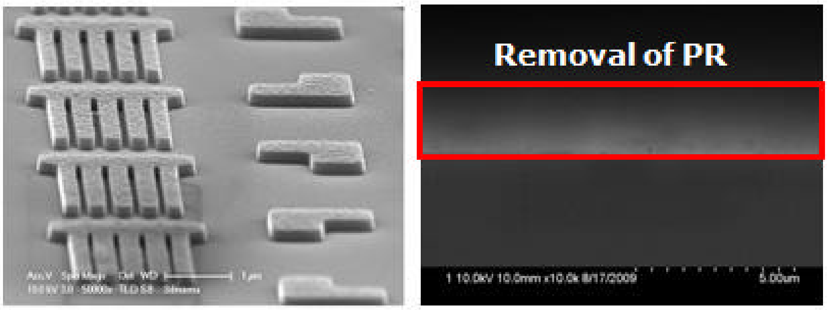


(3-b) After cleaning of BEOL wafer

Figure 3. The SCORR result of BEOL wafer



(4-a) Before cleaning of post ion-implanted wafer



(4-b) After cleaning of post ion-implanted wafer

Figure 4. The SCORR result of post-ion implanted wafer

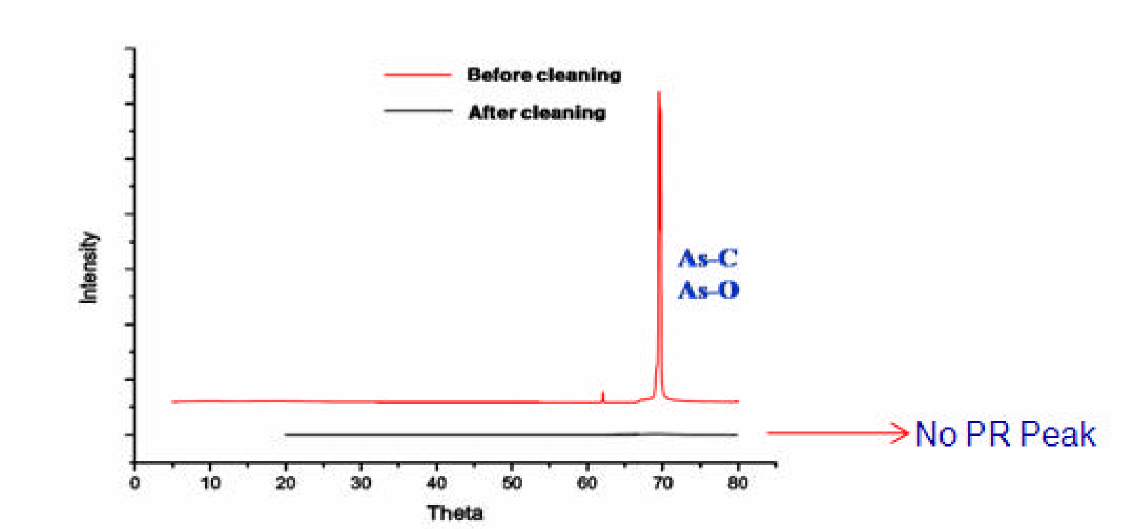
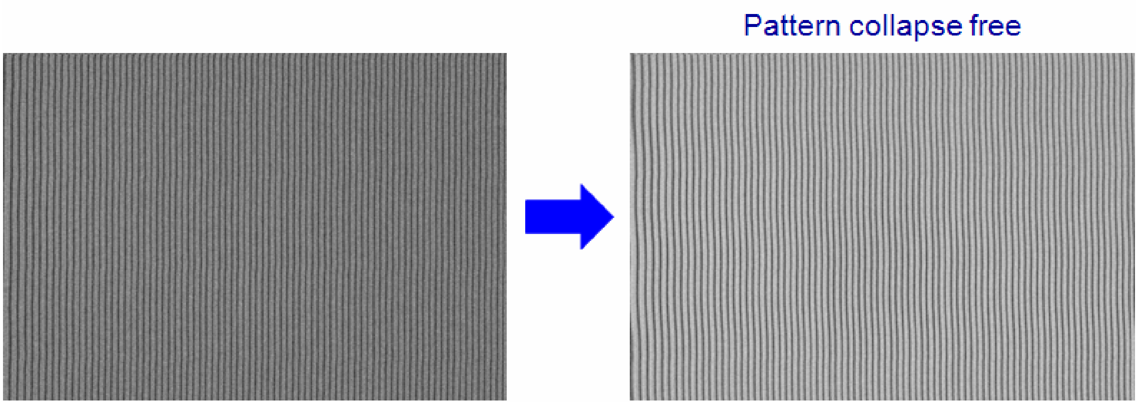


Figure 5. XRD spectrum before and after SCORR of blanket ion implanted wafer



(4-a) Before sc-CO_2 Drying (4-b) After sc-CO_2 Drying

Figure 6. sc-CO_2 Drying result of 20nm-class NAND flash memory pattern wafer

4. Conclusion

Commercial-version SCORR system for cleaning and drying nano-pattern wafers was originally manufactured, and good cleaning and drying results were obtained using it. For the removal of photoresist using sc-CO_2 mixture of homogeneous and transparent phase, appropriate surfactants and solvents were formulated and the reasonable formulation recipes of new mixed cleaning reagents were found. It was seen that the proposed reagent recipes can use at the cleaning conditions below 100°C and 30MPa to uniformly clean the various types of wafers while maintaining a homogeneous supercritical phase during the whole cleaning processing. Based on the good SCORR results obtained from this work, it was found that the SCORR system demonstrated here can be a practical alternative for replacing wet-strip system and partly wet cleaning stations in semiconductor fabrication line in the near future.

5. References

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